REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 94-100, 102, 105-110, 112-116, 119-120, 123, 126-129 and 131 are pending, wherein Claims 94-100, 102, 105-110, 112-116, 119-120, 123, 126-129 and 131 are currently amended, and Claims 101, 103-104, 111, 117-118, 121-122, 124-125, 130 and 132-135 are canceled.

The applicant hereby withdraws a benefit for claiming prior applications. The last sentence originating from the prior applications, to which this application originally claims priority, previously added in the first full paragraph on page 18 is canceled.

The Specification has been amended to correct typographical errors. "um" is amended to "μm".

Response to Claim Rejections under 35 U.S.C. 112

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response To Point 3 of Examiner's opinions

Applicants consider that the specification discloses a passivation layer comprises a topmost oxide layer or a topmost nitride layer.

Applicants teach that a passivation layer 4 comprises an oxide layer or a nitride layer. ~ *see FIG. 2, and lines 1-4 of the third paragraph, in page 18* ~ Furthermore, applicants teach that the insulating layers 5, 14 and 16 over the passivation layer 4 are polymer. ~ *see FIG. 2, lines 5, 7 and 13-15 of the last paragraph, in page 21* ~ Based on the above-mentioned disclosure, applicants do teach the concept that "there could be no nitride layer or oxide layer over a passivation layer". Therefore, it is can be considered that "a passivation layer comprises a topmost nitride layer or a topmost oxide layer of a semiconductor wafer or chip", as claimed in claims 95-96, 107-108, and 126-127. When applicants refer to a topmost nitride layer, for example, it is in reference to a nitride layer that is above any and all other nitride layers. It is not intended to mean a topmost layer as described by the Examiner, i.e., having an exposed or no other layer over its surface.

With regard to claim 102 and reference to a "topmost polymer layer", from FIGS. 6 and 7, applicants teach that there is no other polymer layer over a polymer layer 5. Therefore, the polymer layer 5 of Figs. 6 and 7 can be considered as a topmost polymer layer. The polymer layer 5 may have a metallization structure formed thereon. As a result, applicants do teach that metallization structure is over a topmost polymer layer, as claimed in claim 102.

Response To Point 4 of Examiner's opinions

The claims have been amended to provide proper antecedent basis for the limitation "semiconductor chip or wafer".

Claims 126 and 127, as well as other claims, have been amended to change "insulating layer" to "passivation layer".

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 94-100, 102 and 105

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As currently amended, independent claim 94 is recited below:

94. A semiconductor chip or wafer comprising:
a silicon substrate;
a first metallization structure over said silicon substrate;
a passivation layer over said first metallization structure; and
a second metallization structure over said passivation layer, wherein said second metallization structure comprises a metal layer having a thickness of between 2 and 100 μm, and wherein said second metallization structure connects multiple separate portions of said first metallization structure.

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Section I

Reconsideration of Claim 94 rejected under 35 U.S.C. 102(b) as being anticipated by US5,436,412 to Ahmad et al.

Applicants respectfully assert that the semiconductor chip or wafer claimed in claim 94 patentably distinguishes over the citation by Ahmad et al (US5,436,412).

Ahmad et al teach that an electronic component comprises a metallization structure 24, 34 38, and 44' over a substrate 10. The electronic component further comprises an insulating layer 30, 40 or 50 over the substrate 10, the insulating layer 30 being between the neighboring two patterned metal layers of the metallization structure 24, 34 and 44'. ~ *See FIG. 2 or 3* ~ However, Ahmad et al. fail to teach, hint or suggest that the insulating layer 30, 40 or 50 may be a passivation layer. Those skilled in the art should not come up with the subject matter of "a metallization structure over a passivation layer" because Ahmad et al fail to teach, hint or suggest the subject matter that a passivation layer could be formed over the substrate 10.

Furthermore, Ahmad et al fail to teach, hint or suggest that a metallization structure over a passivation layer connects multiple separate portions of another metallization structure under the passivation layer.

For at least the foregoing reasons, applicants respectfully submit independent claim 94 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 95-100, 102 and 105 patently define over the prior art as well.

Section II

Reconsideration of Claim 94 rejected under 35 U.S.C. 102(e) as being anticipated by US6,417,575 to Harada et al.

Applicants respectfully assert that the semiconductor chip or wafer claimed in claim 94 patentably distinguishes over the citation by Harada et al (US6,417,575).

Harada et al teach that an electronic component comprises a metallization structure 10, 14 and 100 over a semiconductor substrate 1, and a passivation layer 202 over the metallization structure 10, 14 and 100. ~*See FIG. 30 and lines 52-58, col. 24*~ However, Harada et al. fail to teach, hint or suggest that the electronic component further comprises another metallization structure over the passivation layer 202b.

For at least the foregoing reasons, applicants respectfully submit independent claim 94 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 95-100, 102 and 105 patently define over the prior art as well.

Response to Claims 106-110, 112-116 and 119

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As currently amended, independent claim 106 is recited below:

106. A semiconductor chip or wafer comprising:
a silicon substrate;
a first metallization structure over said silicon substrate, wherein said first metallization structure comprises a first contact pad;
a passivation layer over said first metallization structure, wherein an opening in said passivation layer exposes said first contact pad; and

a second metallization structure over said passivation layer, wherein said second metallization structure comprises a gold layer with a thickness of between 2 and 100 μm, wherein said second metallization structure comprises a second contact pad connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different.

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Reconsideration of Claim 106 rejected under 35 U.S.C. 103(a) as being unpatentable over US5,659,201 to Wollesen.

Applicants respectfully assert that the semiconductor chip or wafer claimed in claim 106 patentably distinguishes over the citation by Wollesen (US5,659,201).

Wollesen teaches that an electronic component comprises a first metallization structure 20, 22 and 28 under a passivation layer 23 and 24, and a second metallization structure 71 over the passivation layer 23 and 24. ~ *See FIG. 7* ~

In the latest office action mailed Oct. 28, 2005, Examiner considers that the metallization structure 71 may comprises a contact pad deemed as the left portion of the metallization structure 71. ~ *See lines 15-16, page 8* ~

However, applicants do not think that the metallization structure 71 may comprise a contact pad because Wollesen fails to teach, hint or suggest that the metallization structure 71 may be connected to an external circuitry. Furthermore, this is shown in Wolleson's Fig. 8 in which protective dielectric layer 80 is formed over metallization structure 84. There is no opening in the protective dielectric layer 80 exposing the metallization structure 84. Therefore,

Wollesen fails to teach, hint or suggest that the metallization structure 84 could have a bond pad region because there is no portion of the metallization structure 84 exposed to the outside through an opening in the protective dielectric layer 80 for being joined with an external circuitry.

Furthermore, Wollesen fails to teach, hint or suggest that the metallization structure 71 may comprise a gold layer 71 with a thickness of between 2 and 100 μm. In the latest office action mailed Oct. 28, 2005, Examiner considers that it would have been obvious to one of ordinary skill in art to use or combine (teaching of second reference) in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation.

However, applicants do not consider that the subject matter that "the metallization structure over a passivation layer comprises a gold layer with a thickness of between 2 and 100 μm" is a general condition. If Examiner thinks that the subject matter is a general condition, a prima facie case should be built to support the Examiner's view. Applicants consider that the subject matter that "the metallization structure over a passivation layer comprises a gold layer with a thickness of between 2 and 100 μm" should be patentable, because the subject matter is not shown in any reference.

For at least the foregoing reasons, applicants respectfully submit independent claim 106 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 107-110, 112-116 and 119 patently define over the prior art as well.

Response to Claims 120, 123, 126-129, and 131

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As currently amended, independent claim 120 is recited below:

120. A semiconductor chip or wafer comprising:
a silicon substrate;
a first metallization structure over said silicon substrate, wherein said first metallization structure comprises a first contact pad;
a passivation layer over said first metallization structure, wherein an opening in said passivation layer exposes said first contact pad; and
a second contact pad connected to said first contact pad, wherein said second contact pad comprises a gold layer with a thickness of between 2 and 100 μm and is used to be wirebonded thereto.

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Section I

Reconsideration of Claim 120 rejected under 35 U.S.C. 102(b) as being anticipated by US5,436,412 to Ahmad et al.

Applicants respectfully assert that the semiconductor chip or wafer claimed in claim 120 patentably distinguishes over the citation by Ahmad et al (US5,436,412).

Ahmad et al teach that an electronic component comprises a metallization structure 24, 34 and 44' over a substrate 10. The electronic component further comprises an insulating layer 30, 40 or 50 over the substrate 10, the insulating layer 30 being between the neighboring two patterned metal layers of the metallization structure 24, 34 and 44'. ~ *See FIG. 2 or 3* ~ However, Ahmad et al. fail to teach, hint or suggest that the insulating layer 30, 40 or 50 may be

a passivation layer. Those skilled in the art should not come up with the subject matter of "a metallization structure over a passivation layer" because Ahmad et al fail to teach, hint or suggest the subject matter that a passivation layer could be formed over the substrate 10.

Furthermore, Ahmad et al fail to teach, hint or suggest that a contact pad connected to another pad exposed by an opening in the passivation layer can be used to be wirebonded thereto.

For at least the foregoing reasons, applicants respectfully submit independent claim 120 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 123, 126-129, and 131 patently define over the prior art as well.

Section II

Reconsideration of Claim 120 rejected under 35 U.S.C. 102(e) as being anticipated by US6,417,575 to Harada et al.

Applicants respectfully assert that the semiconductor chip or wafer claimed in claim 120 patentably distinguishes over the citation by Harada et al (US6,417,575).

Harada et al teach that an electronic component comprises a metallization structure 10, 14 and 100 over a semiconductor substrate 1, and a passivation layer 202b over the metallization structure 10, 14 and 100, an opening in the passivation layer 202b exposing a pad 204 of the metallization structure 10, 14 and 100. ~ *See FIG. 30 and lines 52-58, col. 24* ~ However,

Harada et al. fail to teach, hint or suggest that the electronic component further comprises another pad used to be wirebonded thereto, that can be connected to the pad 204.

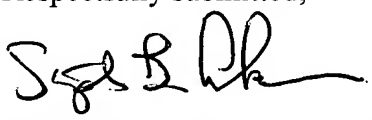
For at least the foregoing reasons, applicants respectfully submit independent claim 120 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 123, 126-129, and 131 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Le not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



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